PCN 14_0066

ADG5233/ADG5234 Data Sheet Changes

Rev. B to Rev. C

This document highlights the performance differences between the Rev.B and Rev.C Transfer for the ADG5233 and ADG5234 Analog Multiplexers.

For full product information and changes to Typical Performance Characteristics plots please refer to the ADG5233/34 Rev.C data sheet.

1. HBM ESD

HBM ESD	Rev B	Rev C	
I/O Port to Supplies	4 kV	8 kV	
I/O Port to I/O Port	1 kV	2 kV	
All other pins	4 kV	8 kV	

2. Datasheet specification changes from Rev. B to Rev. C

Tables 1 to 4 outline a datasheet specification comparison of Rev. B to Rev. C material. The changed specifications are highlighted in red font.

SPECIFICATION CHANGES FROM Rev. B to Rev. C

Table 1. V_{DD} = +15 V \pm 10%, V_{SS} = -15 V \pm 10%, GND = 0 V, unless otherwise noted.

	Rev. B				Rev. C							
Parameter	25°C	−40°C to +85°C	−40°C to +125°C		25°C	−40°C +85°C	to	−40°C to +125°C		Unit	Test Conditions/ Comments	
ANALOG SWITCH												
Analog Signal Range	160		V_{DD} to V_{SS}		160			V_{DD} to V_{SS}		V Ωtyp	$V_S = \pm 10 \text{ V}, I_S = -1 \text{ mA}$	
On Resistance, R _{ON}		250		200			250		200		$V_{DD} = +13.5 \text{ V, } V_{SS} =$	
• ***	200	250		280	200		250		280	Ω max	−13.5 V	
On-Resistance Match Between Channels, ΔR _{ON}	3.5 8	9		10	3.5 8		9		10	Ω typ $Ω$ max	$V_s = \pm 10 \text{ V}, I_s = -1 \text{ mA}$	
On-Resistance Flatness, R _{FLAT}	38	,		10	38		,		10	Ωtyp	$V_S = \pm 10 \text{ V}, I_S = -1 \text{ mA}$	
(ON)	50	65		70	50		65		70	Ω max		
LEAKAGE CURRENTS											$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$	
Source Off Leakage, ls (Off)	±0.02				±0.02					nA typ	$V_S = \pm 10 \text{ V}, V_D = \pm 10 \text{ V}$	
3,,,,,,	±0.1	±0.2	±0.4		±0.1	±0.2		±0.4		nA max		
Drain Off Leakage, I _D (Off)	±0.02				±0.02					nA typ	$V_S = \pm 10 \text{ V}, V_D = \pm 10 \text{ V}$	
Drain On Leakage, ib (Oil)	±0.1	±0.2	±0.4		±0.1	±0.2		±0.4		nA max	V	
Channel On Leakage, I _D (On), I _S (±0.08				±0.08					nA typ	$\pm V_S = V_D = \pm 10 \text{ V}$	
On)	±0.2	±0.3	±0.9		±0.2	±0.3		±0.9		nA max		
DIGITAL INPUTS		_0.5	_0.5					_0.5		THENTIAL		
Input High Voltage, V _{INH}				2					2	V min		
Input Low Voltage, V _{INL} Input Current, I _{INL} or I _{INH}	0.002			8.0	0.002				8.0	V max μΑ typ	$V_{IN} = V_{GND}$ or V_{DD}	
input current, inc or inst	0.002		±0.1		0.002			±0.1		μA max	VIII — VGIND OI VDD	
Digital Input Capacitance, C _{IN}	3				3					pF typ		
Dynamic Characteristics ¹	170				125					ns typ	$R_L = 300 \Omega, C_L = 35 pF$	
Transition Time, transition	210	250		280	160		190		215	ns max	$V_S = 10 \text{ V}$	
ton (EN)	175				145					ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$	
	215 80	255		290	175 125		210		240	ns max ns typ	$V_S = 10 \text{ V}$ $R_L = 300 \Omega, C_L = 35 \text{ pF}$	
t _{OFF} (EN)	100	115		125	155		170		180	ns max	$V_S = 10 \text{ V}$	
Break-Before-Make Time Delay,	60				45					ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$	
to				30					25	ns min	$V_{S1} = V_{S2} = 10 \text{ V}$ $V_S = 0 \text{ V}, R_S = 0 \Omega, C_L =$	
Charge Injection, Q _{INJ}	-0.6				0.4					pC typ	1 nF	
Off Isolation	-75				-76					dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$	
Channel-to-Channel Crosstalk	-80				-87					dB typ	$R_L = 50 \Omega, C_L = 5 pF, f$ = 1 MHz	
–3 dB Bandwidth	205				355					MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$	
Insertion Loss	-6.3				-6.4					dB typ	$R_L = 50 \Omega, C_L = 5 pF, f$ = 1 MHz	
C _s (Off)	4.5				2.8					pF typ	$V_S = 0 V, f = 1 MHz$	
C_D (Off) C_D (On), C_S (On)	10 15				9 13					pF typ pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$ $V_S = 0 \text{ V, } f = 1 \text{ MHz}$	
	13				13					рг цур	$V_{DD} = +16.5 \text{ V}, V_{SS} =$	
POWER REQUIREMENTS											–16.5 V	
lee.	45				45					μA typ	Digital inputs = 0 V or VDD	
I _{DD}	55			70	55				70	μA max	v ∪∪	
l	0.001				0.001					μA typ	Digital inputs = 0 V or V_{DD}	
I _{SS}				1					1	μA max	עטע י	
V_{DD}/V_{SS}			±9/±22					±9/±22		V min/V max	GND = 0 V	

¹ Guaranteed by design, not subject to production test.

Table 2. $VDD = +20V \pm 10\%$, $Vss = -20V \pm 10\%$, GND = 0V, unless otherwise noted.

		Rev.B				Rev	C			
Parameter	25°C	-40°C to +85°C	−40°C to +125°C		25°C	–40°C to +85°C	−40°C to +125°C		Unit	Test Conditions/ Comments
ANALOG SWITCH										
Analog Signal Range			$V_{\text{DD}}toV_{\text{SS}}$				V_{DD} to V_{SS}		V	
0.0	140				140				Ωtyp	$V_S = \pm 15 \text{ V}, I_S = -1 \text{ mA}$
On Resistance, R _{ON}	160	200		230	160	20	0	230	Ω max	$V_{DD} = +18 \text{ V}, V_{SS} = -18 \text{ V}$
On-Resistance Match Between	3.5				3.5				Ωtyp	$V_S = \pm 15 \text{ V, } I_S = -1 \text{ mA}$
Channels, ΔR _{ON}	8	9		10	8		9	10	Ω max	
On-Resistance Flatness, R _{FLAT}	33				33	_	_		Ωtyp	$V_S = \pm 15 \text{ V}, I_S = -1 \text{ mA}$
(ON)	45	55		60	45	5	5	60	Ω max	V -22V/V 22
LEAKAGE CURRENTS										$V_{DD} = +22 \text{ V}, V_{SS} = -22 \text{ V}$
Source Off Leakage, ls (Off)	±0.02				±0.02				nA typ	$V_S = \pm 15 \text{ V}, V_D = \pm 15 \text{ V}$
Source Off Leakage, is (Off)	±0.1	±0.2	±0.4		±0.1	±0.2	±0.4		nA max	
Drain Off Leakage, I _D (Off)	±0.02	.0.2	. 0. 4		±0.02	. 0. 2	. 0. 4		nA typ	$V_S = \pm 15 \text{ V}, V_D = \pm 15 \text{ V}$
5	±0.1	±0.2	±0.4		±0.1	±0.2	±0.4		nA max	$\pm V_S = V_D = \pm 15 \text{ V}$
Channel On Leakage, I _D (On), I _S (±0.08				±0.08				nA typ	T 42 - 40 - 712 4
On)	±0.2	±0.3	±0.9		±0.2	±0.3	±0.9		nA max	
DIGITAL INPUTS										
Input High Voltage, V _{INH}				2				2	V min	
Input Low Voltage, V _{INL}	0.002			0.8	0.002			0.8	V max	\ \ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\
Input Current, I _{INL} or I _{INH}	0.002		±0.1		0.002		±0.1		μΑ typ μΑ max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C _{IN}	3		±0.1		3		±0.1		pF typ	
Dynamic Characteristics ¹									1	
Transition Time, t _{TRANSITION}	170				125				ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
Transition Time, transmon	200	235		260	155	18	0	200	ns max	$V_S = 10 \text{ V}$
ton (EN)	165 200	240		265	145 170	20	0	220	ns typ ns max	$R_L = 300 \Omega, C_L = 35 pF$ $V_S = 10 V$
	80	240		203	125	20	O	220	ns typ	$R_L = 300 \Omega$, $C_L = 35 pF$
t _{OFF} (EN)	95	105		115	155	16	0	170	ns max	V _S = 10 V
Break-Before-Make Time Delay,	50				40				ns typ	$R_L = 300 \Omega, C_L = 35 pF$
t_D				30				20	ns min	$V_{S1} = V_{S2} = 10 \text{ V}$
Charge Injection, Q _{INJ}	0				0.7				pC typ	$V_S = 0 \text{ V}, R_S = 0 \Omega, C_L = 1 \text{ nF}$
Officiation	75				76				dD to on	$R_L = 50 \Omega, C_L = 5 pF, f$
Off Isolation	-75				-76				dB typ	= 1 MHz
Channel-to-Channel Crosstalk	-80				-87				dB typ	$R_L = 50 \Omega, C_L = 5 pF, f$ = 1 MHz
-3 dB Bandwidth	210				370				MHz typ	$R_L = 50 \Omega$, $C_L = 5 pF$
Insertion Loss	-5.5				-5.6				dB typ	$R_L = 50 \Omega, C_L = 5 pF, f$
C _s (Off)	4.5				2.8				pF typ	= 1 MHz V _S = 0 V, f = 1 MHz
C _D (Off)	10				9				pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
C_D (On), C_S (On)	15				13				pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
POWER REQUIREMENTS										$V_{DD} = +22 \text{ V}, V_{SS} = -22 \text{ V}$
	50				50				μA typ	Digital inputs = 0 V or
IDD	70			110	70			110	μA max	V_{DD}
				. 10				. 10	'	Digital inputs = 0 V or
Iss	0.001				0.001				μA typ	V _{DD}
V 0/			.0/.22	1			.0/.22	1	μA max	CND OV
V_{DD}/V_{SS}	<u> </u>		±9/±22		<u> </u>		±9/±22		V min/V max	GND = 0 V

¹ Guaranteed by design, not subject to production test.

Table 3. $V_{DD} = +12V \pm 10\%$, $V_{SS} = 0V$ GND = 0 V, unless otherwise noted.

	Rev.B				Rev.	С				
Parameter	25°C	–40°C to +85°C	−40°C to +125°C		25°C	−40°C to +85°C	−40°C t +125°C		Unit	Test Conditions/ Comments
ANALOG SWITCH Analog Signal Range			0 V to V _{DD}	•			0 V to V	OD .	V	
On Resistance, R _{ON}	360				360				Ωtyp	$V_S = 0 V \text{ to } 10V, I_S = -1 \text{ mA}$
Off nesistatice, non	500	610		700	500	610		700	Ω max	$V_{DD} = +10.8V, V_{SS} = 0$
On-Resistance Match Between	5.5				5.5				Ωtyp	$V_S = 0 V \text{ to } 10V, I_S = -1 \text{ mA}$
Channels, ΔR _{ON}	20	21		22	20	21		22	Ω max	
On-Resistance Flatness, R _{FLAT}	170	225		270	170	225		270	Ωtyp	$V_s = 0 V$ to 10V, $I_s = -1 \text{ mA}$
	280	335		370	280	335		370	Ω max	$V_{DD} = 13.2 \text{ V}, V_{SS} =$
LEAKAGE CURRENTS										0V
Source Off Leakage, ls (Off)	±0.02				±0.02				nA typ	$V_s = 1V/10V, V_D = +10 V/1V$
3,	±0.1	±0.2	±0.4		±0.1	±0.2	±0.4		nA max	
Drain Off Leakage, I _D (Off)	±0.02				±0.02				nA typ	$V_s = 1V/10V, V_D = +10 V/1V$
Drain on Leanage, is (on)	±0.1	±0.2	±0.4		±0.1	±0.2	±0.4		nA max	110 47 14
Channel On Leakage, I_D (On), I_S (±0.08				±0.08				nA typ	$\pm V_S = V_D = 1 \text{ V}/10 \text{V}$
On)	±0.2	±0.3	±0.9		±0.2	±0.3	±0.9		nA max	± V 3 = V D = 1 V /10 V
DIGITAL INPUTS Input High Voltage, V _{INH} Input Low Voltage, V _{INL} Input Current, I _{INL} or I _{INH} Digital Input Capacitance, C _{IN}	0.002		±0.1	2 0.8	0.002		±0.1	2 0.8	V min V max μA typ μA max pF typ	$V_{IN} = V_{GND} \text{ or } V_{DD}$
DYNAMIC CHARACTERISTICS ¹									рг тур	
	235				165				ns typ	$R_L = 300 \Omega, C_L = 35$
Transition Time, trransition	295	365		410	215	260		300	ns max	pF V _S = 8 V
	240				200				ns typ	$R_L = 300 \Omega, C_L = 35$
ton (EN)	305	380		430	245	305		350	ns max	pF V _S = 8 V
	70	300		.50	130	303		330	ns typ	$R_L = 300 \Omega, C_L = 35$
t _{OFF} (EN)	90	105		115	165	180		200	ns max	pF V _S = 8 V
Break-Before-Make Time Delay,	125	103		113	85	100		200	ns typ	$R_L = 300 \Omega, C_L = 35$
t _D	123			65	03			45	ns min	pF $V_{S1} = V_{S2} = 8 \text{ V}$
Charge Injection, Q _{INJ}	0			05	0			73	pC typ	$V_S = 6 \text{ V}, R_S = 0 \Omega, C_L$
Off Isolation	-75				-76				dB typ	= 1 nF $R_L = 50 \Omega$, $C_L = 5 pF$,
Channel-to-Channel Crosstalk	-80				-87				dB typ	f = 1 MHz $R_L = 50 \Omega, C_L = 5 \text{ pF},$
–3 dB Bandwidth	172				260				MHz typ	f = 1 MHz $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$
Insertion Loss	-8.7				-9				dB typ	$R_L = 50 \Omega$, $C_L = 5 pF$,
C_s (Off) C_D (Off) C_D (On), C_s (On)	5 11 16				3 10 14				pF typ pF typ pF typ	f = 1 MHz $V_S = 0 \text{ V, } f = 1 \text{ MHz}$ $V_S = 0 \text{ V, } f = 1 \text{ MHz}$ $V_S = 0 \text{ V, } f = 1 \text{ MHz}$
POWER REQUIREMENTS										V _{DD} = 13.2
I _{DD}	40 50			6 5	40			65	μA typ	Digital inputs = 0 V or V_{DD}
VDD . Guaranteed by design not subject	50		9/40	65	50		9/40	65	μA max V min/V max	GND = 0 V, Vss=0V

 $_{\mbox{\scriptsize 1}}\,\mbox{\scriptsize Guaranteed}$ by design, not subject to production test.

Table 4. V_{DD} = +36V ± 10%, V_{SS} = 0V GND = 0 V, unless otherwise noted.

	Rev.B				Rev. C			
Parameter	25°C	−40°C to +85°C	–40°C to +125°C	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/ Comments
ANALOG SWITCH			0.1/+1/			0.77+-77	V	
Analog Signal Range	140		0 V to V _{DD}	1.40		0 V to V _{DD}	,	$V_S = \pm 10 \text{ V, } I_S = -1$
On Resistance, Ron	140			140			Ωtyp	mA
·	170	215	245	170	215	245	Ω max	$V_{DD} = +13.5 \text{ V}, V_{SS} = -13.5 \text{ V}$
On-Resistance Match Between	3.5			3.5			Ωtyp	$V_S = \pm 10 \text{ V, } I_S = -1 \text{ mA}$
Channels, ΔR _{ON}	8	9	10	8	9	10	Ω max	IIIA
On-Resistance Flatness, R _{FLAT}	35			35			Ωtyp	$V_S = \pm 10 \text{ V, } I_S = -1 \text{ mA}$
(ON)	50	60	65	50	60	65	Ω max	IIIA
LEAKAGE CURRENTS								$V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$
	±0.02			±0.02			nA typ	$V_S = \pm 10 \text{ V}, V_D =$
Source Off Leakage, ls (Off)	±0.02	±0.2	±0.4	±0.02	±0.2	±0,4	nA max	±10 V
	±0.02	±0.2	±0.4	±0.02	±0.2	±0.4	nA typ	$V_S = \pm 10 \text{ V}, V_D =$
Drain Off Leakage, l₀ (Off)	±0.02	±0.2	±0.4	±0.02	±0.2	±0,4	nA max	±10 V
Channel On Leakage, I _D (On), I _S (±0.08			±0.08			nA typ	$\pm V_S = V_D = \pm 10 \text{ V}$
On) DIGITAL INPUTS	±0.2	±0.3	±0.9	±0.2	±0.3	±0.9	nA max	
Input High Voltage, V _{INH}			2			2	V min	
Input Low Voltage, V _{INL} Input Current, I _{INL} or I _{INH}	0.002		0.8	0.002		0.8	V max μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1			±0.1	μA max	VIN — VGND OI VDD
Digital Input Capacitance, C _{IN} Dynamic Characteristics ¹	3			3			pF typ	
•	205			155			ns typ	$R_L = 300 \Omega, C_L = 35$
Transition Time, t _{TRANSITION}	255	275	290	200	215	230	ns max	pF V _S = 10 V
	200	2/3	270	180	213	250	ns typ	$R_L = 300 \Omega$, $C_L = 35$
t _{on} (EN)	240	265	290	215	235	250	ns max	pF V _S = 10 V
	85	203	270	150	255	250	ns typ	$R_L = 300 \Omega$, $C_L = 35$
t _{OFF} (EN)	115	115	115	190	190	190	ns max	pF V _S = 10 V
Break-Before-Make Time Delay,	65	113	113	50	150	150	ns typ	$R_L = 300 \Omega$, $C_L = 35$
t _D	03		35	30		25	ns min	pF $V_{S1} = V_{S2} = 10 \text{ V}$
Charge Injection, Q _{INJ}	-0.6		33	0.5		23	pC typ	$V_S = 0 V$, $R_S = 0 \Omega$, C_L
Off Isolation	-75			-76			dB typ	= 1 nF $R_L = 50 \Omega, C_L = 5 pF,$
							, ,	f = 1 MHz $R_L = 50 \Omega, C_L = 5 \text{ pF},$
Channel-to-Channel Crosstalk	-80 100			-87			dB typ	f = 1 MHz
–3 dB Bandwidth	190			275			MHz typ	$R_L = 50 \Omega, C_L = 5 pF$ $R_L = 50 \Omega, C_L = 5 pF,$
Insertion Loss	-5.9			-6.2			dB typ	f = 1 MHz
C_S (Off) C_D (Off)	4.5 10			2.8 9			pF typ pF typ	$V_S = 0 V, f = 1 MHz$ $V_S = 0 V, f = 1 MHz$
C_D (On), C_S (On)	15			13			pF typ	$V_S = 0 \text{ V, } f = 1 \text{ MHz}$
POWER REQUIREMENTS								V _{DD} = +16.5 V, V _{SS} = -16.5 V
lop	80			80			μA typ	Digital inputs = 0 V or V_{DD}
	100		130	100		130	μA max	
VDD . Guaranteed by design not subject			Sep-40			Sep-40	V min/V max	GND = 0 V, Vss=0V

 $_{\mbox{\scriptsize 1}}$ Guaranteed by design, not subject to production test.